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EXAMINER	
SHAAWAT, MUSSA	
ART UNIT	**PAPER NUMBER**
2128	

DATE MAILED: 05/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/819,773	GAUTHIER ET AL.	
	Examiner	Art Unit	
	Mussa A. Shaawat	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,9-13,15-19,23 and 27-34* is/are rejected.

7)☐ Claim(s) *5-8,20-22,24-26 and 35-37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/28/03, 3/28/01 M.S.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This application has been examined.

2. Claims 1-37 have been examined.

Claim Interpretation

3. Claim 1 – The board model is interpreted as being a software model. The package model is being interpreted as being a software model of semiconductor devices. The chip model is being interpreted as being a software model of the chip.

4. Claim 4 – The Bump and Grid" is interpreted as "ball and Grid" also.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 14 is rejected under 35 U.S.C. 102(b) as being anticipated by Herrell et al ("Modeling of Power Distribution Systems for High-Performance Microprocessors", IEEE, 1999), herein referred to as Herrell.

7. As per claim 14, Herrell teaches modeling a power converter, modeling a board, modeling a package, and modeling a chip model (Abstract; page 240, section I 2nd and 6th paragraph; section II, 2nd paragraph and Fig. 2).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being obvious over Dennis J. Herrell et al ("Modeling of Power Distribution Systems for High-Performance Microprocessors", IEEE, 1999), herein referred to as Herrell in view of Hiroshi Shimamori (US 5,737,202), herein referred to as Shimamori.

10. As per claim 1 Herrell discloses a power converter model, a board model, a package model, and a chip model (Abstract; page 240, section I 2nd and 6th paragraph; section II, 2nd paragraph and Fig. 2).

Herrell does not expressly disclose the plurality of the power converter models. Shimamori discloses the plurality of the power converters (Fig 1, items 12, 13, and 23). Shimamori does not teach implementation of the converters in a model. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with Shimamori to provide models of power converters.

11. As per claim 2 and 3 Herrell does not expressly disclose the plurality of DC-to-DC converter models and also four DC-to-DC converter models. Shimamori teaches a plurality of DC-to-DC converters (Fig. 1, item 12 and 13) and four DC to Dc converters (Fig. 5, items 56-59). It would have been obvious to one of ordinary skill in the art at the

time of the invention was made to modify the teachings of Herrel with Shimamori to provide models of power converters.

12. Claims 4, 9-13, 15-19, 23, and 27-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herrell in view of Shimamori and further in view of Anderson.

13. As per claim 4 Herrell teaches the plurality of bump and grid models (Page 241, Section II 3rd paragraph), but it fails to teach the plurality of section models and plurality of channel models. Anderson et al (herein referred to as Anderson), US 6385565, teaches about the plurality of section models and the plurality of channel models (Fig. 3A, column 8 lines 33-40, column 9 lines 63-65). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with the teachings of Anderson in order to get an accurate model.

14. As per claim 9 Herrell fails to teach the plurality of section models arranged in an interconnecting grid. Anderson teaches about section grids arranged in an interconnecting grid (Fig 3A, column 8 lines 33-40, column 9 lines 63-65). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with the teachings of Anderson in order to analyze the noise distribution and to get realistic current distribution and design the power system capable of delivering stable power.

15. As per claim 10 Herrell fails to teach the interconnecting grid is generally square shaped. Anderson teaches about interconnecting grid is square shaped (Fig 3A). It would have been obvious to one of ordinary skill in the art at the time of the invention

was made to modify the teachings of Herrell with the teachings of Anderson in order to simplify the calculation for better and efficient simulation.

16. As per claim 11 Herrell fails to teach the plurality of section models comprises nine section models. Anderson teaches the nine section models(Fig. 3A, column 8 lines 33-40). It is an 8x8 grid, which comprises 9 section models. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with the teachings of Anderson in order to analyze the noise distribution and to get realistic current distribution and design the power system capable of delivering stable power.

17. As per claim 12 Herrell fails to teach the plurality of the section models are arranged in a three section by three-section grid. Anderson teaches 8x 8 section grid (Fig. 3A, column 8 lines 33-40) which comprises the 3x3 section grid. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with the teachings of Anderson by selecting any section grid from 1x1 to 8x8 to simplify calculation for better and efficient simulation.

18. As per claim 13 Herrell to teach the plurality of channel models comprises ten section models. However, "Official Notice" has been taken by the examiner that any number of section models can be used to analyze a complex circuit for better and efficient simulation.

19. As per claim 15 Herrell discloses modeling a power converter, modeling a board, modeling a package, and modeling a chip (Abstract; page 240, section I 2nd and 6th paragraph; section II, 2nd paragraph and Fig. 2).

Herrell does not expressly disclose modeling the plurality of the power converters. Shimamori discloses the plurality of the power converters (Fig 1, items 12, 13, and 23).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with Shimamori to provide models of power converters.

20. As per claim 16 Herrell does not expressly disclose the plurality of power converters comprises four DC-to-DC power converters. Shimamori teaches the four DC-to-DC converters (Fig. 5, items 56-59). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrel with Shimamori to provide models of power converters.

21. As per claim 17 Herrell teaches about modeling a plurality of bump and grid components (Page 241, Section II 3rd paragraph), but it fails to teach modeling a plurality of chip sections and plurality of chip channels. Anderson teaches the chip section models and the chip channel models (Fig. 3A, column 8 lines 33-40, column 9 lines 63-65). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with the teachings of Anderson in order to get an accurate model.

22. As per claim 18 Herrell fails to teach modeling a plurality of chip section forms generally a square shaped grid. Anderson teaches about chip grid is a square shaped (Fig 3A). It would have been obvious to one of ordinary skill in the art at the time of the

invention was made to modify the teachings of Herrell with the teachings of Anderson in order to simplify the calculation for better and efficient simulation.

23. As per claim 19 Herrell fails to teach the generally square shaped grid comprises a three section by three-section grid. Anderson teaches 8x 8 section grid (Fig. 3A, column 8 lines 33-40) which comprises the 3x3 section grid. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with the teachings of Anderson by selecting any section grid from 1x1 to 8x8 to simplify calculation for better and efficient simulation.

24. As per claim 23 Herrell in view of Shimamori and in further view of Anderson as applied to claim 4 teaches all the subject matter of claim 23.

25. As per claim 27 Herrell fails to teach the plurality of section models are arranged in an interconnecting grid. Anderson teaches about section grids arranged in an interconnecting grid (Fig 3A, column 8 lines 33-40, column 9 lines 63-65). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with the teachings of Anderson in order to analyze the noise distribution and to get realistic current distribution and design the power system capable of delivering stable power.

26. As per claim 28 Herrell fails to teach the interconnecting grid is square shaped. Anderson teaches about interconnecting grid is square shaped (Fig 3A). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with the teachings of Anderson in order to simplify the calculation for better and efficient simulation.

27. As per claim 29 Herrell fails to teach the plurality of section models comprises nine section models. Anderson teaches the nine section models (Fig. 3A, column 8 lines 33-40). It is an 8x8 grid, which comprises 9 section models. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with the teachings of Anderson in order to analyze the noise distribution and to get realistic current distribution and design the power system capable of delivering stable power.

28. As per claim 30 Herrell fails to teach the plurality of the section models are arranged in a three section by three-section grid. Anderson teaches 8x 8 section grid (Fig. 3A, column 8 lines 33-40) which comprises the 3x3 section grid. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with the teachings of Anderson by selecting any section grid from 1x1 to 8x8 to simplify calculation for better and efficient simulation.

29. As per claim 31 Herrell in view of Shimamori and in further view of Anderson as applied to claim 23 teaches all the subject matter of claim 31.

30. As per claim 32, claim 32 is a method claim containing the same subject matter as the apparatus of claim 23. Claim 32 is rejected on the same basis as claim 23.

31. As per claim 33 Herrell fails to teach modeling a plurality of chip sections forms a generally square shaped grid. Anderson teaches about interconnecting grid is square shaped (Fig 3A). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with the teachings of Anderson in order to simplify the calculation for better and efficient simulation.

32. As per claim 34 Herrell fails to teach the generally square shaped grid is a three section by three-section grid. Anderson teaches 8x 8 section grid (Fig. 3A, column 8 lines 33-40) which comprises the 3x3 section grid. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Herrell with the teachings of Anderson by selecting any section grid from 1x1 to 8x8 to simplify calculation for better and efficient simulation.

Allowable Subject Matter

33. Claims 5-8, 20-22, 24-26, and 35-37 are objected to as being dependent upon a rejected base claim (and assuming all other rejections are traversed), but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

34. Applicant's arguments have been fully considered but they are not persuasive.

In the remarks, the applicant argues in substance that; A) Herrell fails to disclose modeling a power converter; B) Herrell fails to disclose means for modeling a power converter model; C) Herrell and Shimamori are not properly combinable to reject claim 1.

In response to A) Herrell discloses techniques for building models and simulating the response of power distribution systems for high-performance microprocessors (see Abstract). In addition Herrel discloses the design of the power system capable of delivering stable performance to such stringent demands, requires careful optimization

of various components: switching regulator (dc-dc converter) i.e. power converter, ... package-including decoupling capacitors" (see Section I. Introduction 2nd paragraph). Therefore, Herrell meets the scope of the claimed limitation "modeling a power converter".

In response to B) Herrell discloses, "a practical approach to modeling of power systems is base on the well-known partial element equivalent circuit (PEEC) method. The attractive feature of this approach is that the geometry of the power supply network can be portioned into section for which the partial RLC parameters can be found and used to construct an equivalent Spice circuit of the entire structure i.e. Spice is a means to model a power converter model" (see Section I. Introduction 4th paragraph). Therefore, Herrell meets the scope of the claimed limitation "means for modeling a power converter model".

In response to C) the examiner contends that the motivation to combine Herrell and Shimamori is proper and in accordance with MPEP guidelines for the following reasons. MPEP 2143.01 Suggestion or Motivation To Modify the References first recites:

"There are three possible sources for a motivation to combine references: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art." In re Rouffet, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998)

In this case the examiners rejection first addresses the nature of the problem to be solved, namely, relates to a method for modeling a power system of a microprocessor chip, comprising: modeling a plurality of package model components; modeling a plurality of chip sections that receives an output from the plurality of package model components; and modeling

a plurality chip channels that interconnect the plurality of chip sections, relative to the teachings in the prior art. The examiner references the prior art (Herrell), which discloses SPICE (one of the many available simulations tools) to simulate and model a power distribution system for high performance microprocessors, (see Abstract, et-seq.). Other prior art cited by the examiner such as Shimamori et al similarly discusses redundant power supply system, which includes plurality of power converters such as AC-DC and DC-DC (see Abstract, et-seq). Here, the examiner has established that the market is competitive (crowded), with many known tools to simulate and model power distribution systems in the market place as would be easily recognized by a person skilled in the art. Therefore, in suggesting a motivation to combine, the examiner specifically focused his motivation on the knowledge of persons of ordinary skill in the art. More specifically, that a skilled artisan would have made an effort to become aware of what capabilities had been developed in the market place, and hence would have knowingly modified Herrell with the teachings of Shimamori. MPEP 2144 Sources of Rationale Supporting a Rejection Under 35 U.S.C. 103 recites:

> "The rationale to modify or combine the prior art does not have to be expressly stated in the prior art; the rationale may be expressly or impliedly contained in the prior art or it may be reasoned from knowledge generally available to one of ordinary skill in the art, established scientific principles, or legal precedent established by prior case law. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). See also In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000) (setting forth test for implicit teachings); In re Eli Lilly & Co., 902 F.2d 943, 14 USPQ2d 1741 (Fed. Cir. 1990) (discussion of reliance on legal precedent); In re Nilssen, 851 F.2d 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988) (references do not have to explicitly suggest combining teachings)"

The examiner has simply asserted that a skilled artisan tasked with solving the problem of modeling a power system of a microprocessor chip, comprising: modeling a plurality of package model components; modeling a plurality of chip sections that receives an output

from the plurality of package model components; and modeling a plurality chip channels that interconnect the plurality of chip sections (i.e. as taught by Herrell), from a redundant power supply system, which includes plurality of power converters such as AC-DC and DC-DC (i.e. as taught by Shiamori), and further having access to the teachings of Herrell and Shimamori, would have knowingly modified the teachings of Herrell, with the teachings of Shimamori in order to gain the advantage of reduced cost and development time. Specifically, a skilled artisan working in this obviously competitive environment would have made an effort to become aware of what capabilities had already been developed in the market place, and hence would have been aware of, and known to seek out the relative teachings of the problem to be solved. Namely, the teachings of Herrell and Shimamori.

MPEP 2143.01 Suggestion or Motivation To Modify the References further recites the following supporting rational:

> Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. **"The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art."** In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000).

The examiner therefore appears to have established an implicit showing that in view of the combined teachings of the prior art, the relative knowledge of one skilled in the art, and in particular, the nature of the problem to be solved, there exists an obvious motivation to combine the references as noted above.

In light of the foregoing arguments, the 35 USC 102 rejection is hereby sustained.

35. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

36. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yip et al (US5,694,344) A method of electrically modeling a semiconductor package.

Communication

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mussa A Shaawat whose telephone number is (571)

272-3785. The examiner can normally be reached on Monday-Friday (8:30am to 5:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean R Homere can be reached on (571) 272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mussa Shaawat
Patent Examiner
April 14, 2005

JEAN R. HOMERE
PRIMARY EXAMINER